


|  |                           |           |       |
|--|---------------------------|-----------|-------|
|  <div data-bbox="491 98 539 264" style="display: inline-block; vertical-align: middle; text-align: center;"> <b>I</b><br/> <b>Q</b><br/> <b>R</b> </div> | IBIS<br>QUALITY<br>REPORT | date      | 1 (8) |
|  |                           | 11-Jun-14 |       |

## IBIS Quality Report

|                |                       |
|----------------|-----------------------|
| Company:       | STMicroelectronics    |
| IBIS file name | m24c04_fa1_mlp2x3.ibs |
| IBIS Version:  | 4.0                   |

|  |                            |           |       |
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# 1. MODELING

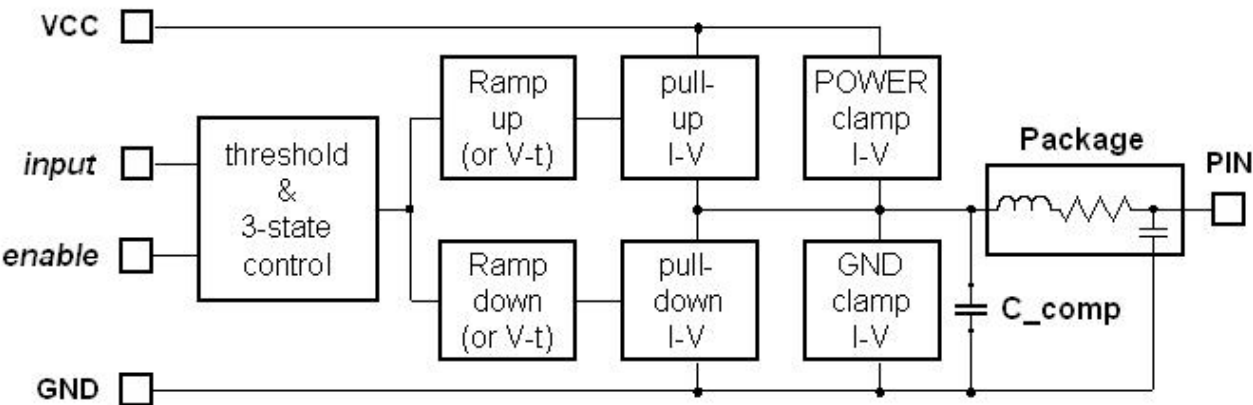
IBIS (I/O, Buffer, Information, Specification) provide a standardized way, officially EIA standard 656-A-1999 and IEC 62014-1, to model behaviorally a digital component input, output and I/O buffers.

## 1.1 Component description

| Component reference                                | Technology     | Component description   |
|--|----------------|---|
| M24C01/02/04-W<br>M24C01/02/04-R<br>M24C01/02/04-F | CMOS<br>F8H/P4 | The M24C01/02/04 is a 1/2/4-Kbit I <sup>2</sup> C-compatible EEPROM (Electrically Erasable PROgrammable Memory).<br>The M24C01/02/04-W can be accessed (Read and Write) with a supply voltage from 2.5V to 5.5V, the M24C01/02/04-R can be accessed with a supply voltage from 1.8V to 5.5V, and the M24C01/02/04-F can be accessed with a supply voltage from 1.7V to 5.5V |

## 1.2 Modeling conditions

|                |                              |
|----------------|------------------------------|
| Simulator used | AMS 2010.1 (Mentor Graphics) |
|----------------|------------------------------|



**Figure 1:** IBIS model generic structure

| conditions              | Typical | Minimum | Maximum |
|-------------------------|---------|---------|---------|
| Temperature [C°]        | 25      | -40     | 85      |
| Voltage Supply * [Volt] | 1.8     | 1.7     | 2.0     |
| Process setting         | nom     | weak    | strong  |

|  |                            |           |       |
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| * Different Voltage Reference<br>(only if Voltage Supply is not present) | Typical | Minimum | Maximum |
|--|---------|---------|---------|
| Pullup Voltage Reference [Volt]  | -       | -       | -       |
| Pulldown Voltage Reference [Volt]  | -       | -       | -       |
| Power Clamp Voltage Reference [Volt]                                     | -       | -       | -       |
| GND Clamp Voltage Reference [Volt]                                       | -       | -       | -       |

| Model names<br>(of Component) | Model Type     | C_comp (typ, min, max)                       |
|-------------------------------|----------------|--|
| mod_sda                       | I/O_Open_Drain | 3.856pF (typ), 3.682pF(min) , 4.038pF (max)  |
| mod_scl                       | Input          | 1.763pF (typ), 1.683pF (min) , 1.933pF (max) |
| mod_wc                        | Input          | 1.763pF (typ), 1.683pF (min) , 1.933pF (max) |
| mod_en                        | Input          | 1.763pF (typ), 1.683pF (min) , 1.933pF (max) |

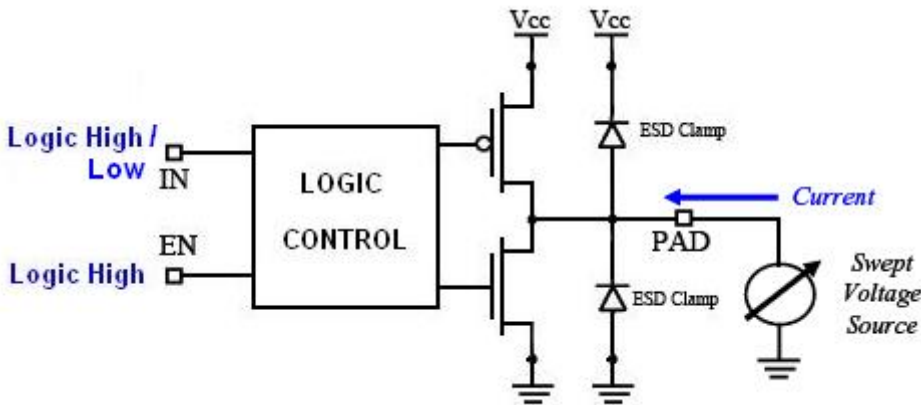
| Model names<br>(of Component) | Threshold and Vmeas    | Timing parameters (if used)    |
|-------------------------------|------------------------|--------------------------------|
| mod_scl/wc/en                 | Vinl=0.54V , Vih=1.26V |                                |
| mod_sda                       | Vmeas=9.00V            | Rref=1k, Cref=10pF, Vref=1.80V |

| Package | description/comment            |
|---------|--------------------------------|
| MLP 2x3 | 8 lead micro leadframe outline |

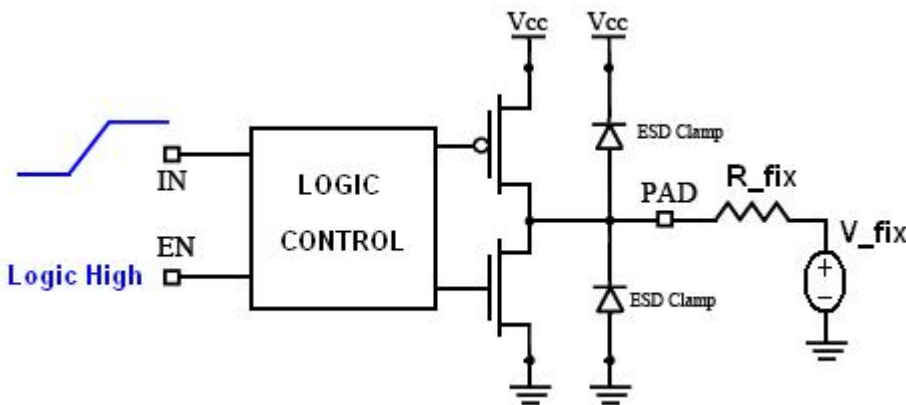
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### 1.3 Circuit for data extraction

The I-V data are extracted by simulations using the simulation setup shown in figure 2 below. This model is an I/O model, other model type derived from this structure. For more accurate modeling, certain combinations of V-T tables are recommended (with exception of Input-only model types) using the simulation setup shown in figure 3, with load conditions specified.



**Figure 2:** Simulation Setup to extract **I/V** data from I/O model type



**Figure 3:** Simulation Setup to extract **V/T** data from I/O model type (see also Table 1)

| V/T data condition extractions | Load conditions            |
|--------------------------------|----------------------------|
| Rising waveform                | R_fix=50 Ohm, V_fix= 0 V   |
| Rising waveform                | R_fix=50 Ohm, V_fix= 1.8 V |
| Falling waveform               | R_fix=50 Ohm, V_fix= 1.8 V |
| Falling waveform               | R_fix=50 Ohm, V_fix= 0 V   |

**Table 1:** V/T curve extraction load conditions

|  |                            |           |       |
|--|----------------------------|-----------|-------|
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## 2. IBISCHK5 CHECK

The created IBIS model must be checked using IBISCHK5 parser to ensure that the syntax is correct. The result of the check is showed in the next section with some comments (optional).

### 2.1 Result Check by IBISCHK5

*IBISCHK5 V5.0.4*

*Checking m24c04\_fa1\_mlp2x3.ibs for IBIS 4.2 Compatibility...*

*NOTE (line 302) - Pulldown Maximum data is non-monotonic*

*NOTE (line 303) - Pulldown Typical data is non-monotonic*

*NOTE (line 303) - Pulldown Minimum data is non-monotonic*

*Errors : 0*

*Warnings: 0*

*File Passed*

|   |
|---|
| <b>Adding comments about the Warning or Note:</b>   |
| The output check contains some Note about non-monotonic data of I-V curves, but they are not indicative of problems inside the model. |

|  |                            |           |       |
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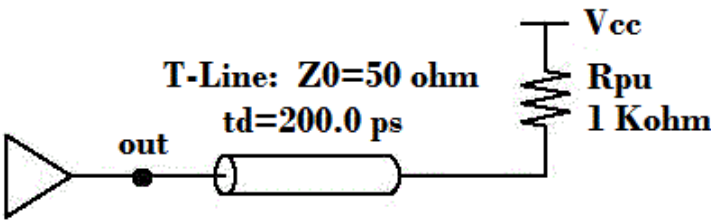
### 3. FUNCTIONAL CHECK

The created IBIS model must be compared with the Original Buffer circuit. The signal outputs, in the same load conditions ( Figure 4), must match. These output comparisons are presented in TYP, MIN and MAX condition. This section cannot be defined for Input and Terminator model type, because they are input-only model types.

| How well results are matched?   | Put “X” into the right filed |
|---|------------------------------|
| Curves shape match correctly, but there is a little time translation.                               |                              |
| Curves shape match correctly, but there is a mismatch into the Overshoot and/or Undershoot regions. |                              |
| Curves match well.  | X                            |

#### 3.1 Functional verification

Circuit used for output comparison results is illustrated in figure 4.



**Figure 4:** Circuit used for functional check

|  |                     |           |       |
|--|---------------------|-----------|-------|
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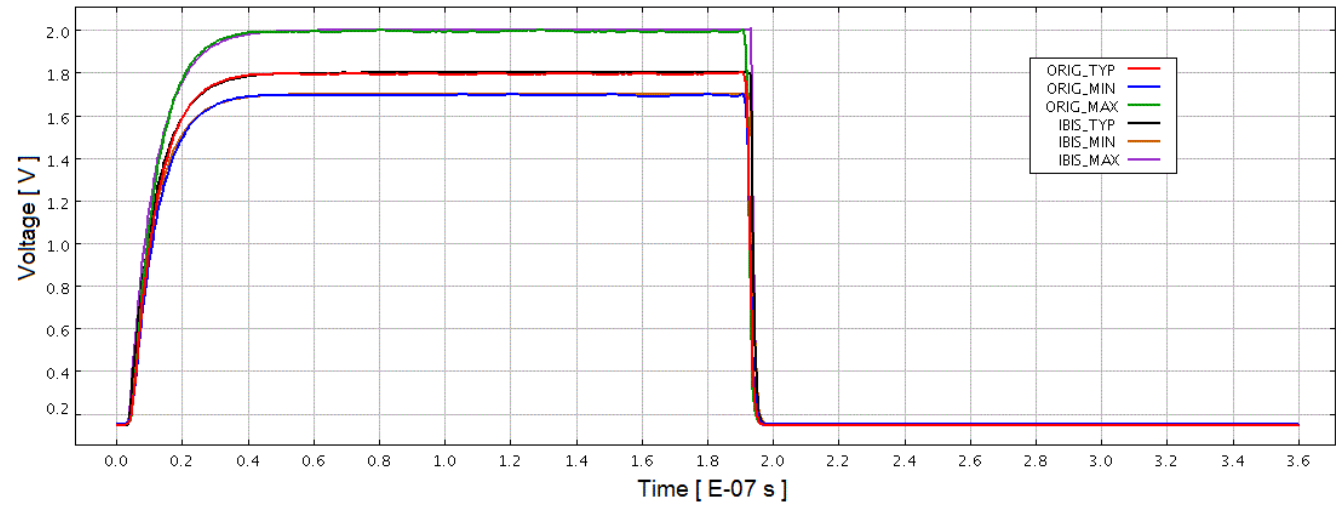


Figure 5: IBIS vs Eldo comparison results of “mod\_sda” Model

Output Comparisons:

|  |
|--|
| <b>Adding comments about the comparison:</b> |
|  |

#### 4. EXTRA INFORMATION

This section can contains other extra informations, to explain some other features of peculiar IBIS model

| Other specifications | description |
|----------------------|-------------|
|                      |             |